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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/737,218	12/14/2000	Robert D. Norman	703.070US2	1359

7590 12/19/2002

Schwegman, Lundberg, Woessner & Kluth, P.A.
P.O. Box 2938
Minneapolis, MN 55402

EXAMINER
PEIKARI, BEHZAD

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

2186

Office Action Summary	Application No. 09/737,218	Applicant(s) NORMAN ET AL.	
	Examiner B. James Peikari	Art Unit 2186	

The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *[telephone interview of Sept. 23, 2002]* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,25,47,55-59 and 61* is/are pending in the application.

4a) Of the above claim(s) *25,47,55-59 and 61* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☒ Interview Summary (PTO-413) Paper No(s). 5 .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Claims 25, 47, 55-59 and 61 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected inventions, there being no allowable generic or linking claim. Election was made **without** traverse by Dan Kluth (#32,146) during a telephone conversation on September 23, 2002.

Specification

2. The disclosure is objected to because of the following minor informalities:

(a) The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed, including the critical claim feature "address assignment".

(b) On page 1, the parent application information should be updated, i.e., "now U.S. Patent No. 6,175,891".

(c) On page 8, "Figures 12A-12N" should be rewritten to describe each claim individually.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al., U.S. 5,617,537.

Yamada et al. teach the present invention with a memory system comprising: A plurality of memory devices (*21, e.g., 21-1, 21-2, and 21-3*), with each memory device comprising

(a) an array of memory cells (*each memory 21 is made up of memory cells*);

(b) an addressing circuitry operatively coupled to the array of the memory cells, wherein the addressing circuitry is capable of providing addresses to the array of memory cells (*note "The distributed shared memories are assigned global addresses common to all processor modules", in the abstract and the "object ID" used throughout – "the destination of a message is specified by the object ID"*);

(c) a memory device bus interface (*there are several for each device 21 – one to interface with the system bus, namely coupler 22, and one to interface with the multiprocessor communication lines, namely adaptor 24, and one to provide protection from either route, namely protector 23*);

(d) a command decoder which decodes commands at the memory device bus interface (), including an address assign command (*30*); and

(e) a local address storage circuitry which stores a local address for identifying the storage circuitry's single associated memory device once the address

assign command is decoded by the command decoder (*the local address, as well as the addresses of other devices, is stored in each PM in map area 21M*); and

(f) a memory controller having a controller bus interface coupled to the memory device bus interface, with the memory controller providing the local address to be stored in the local address storage circuitry of the memory device of the memory system together with the address assign command (*see below*).

As for the claimed use of a system bus for performing the functions above, as in claims 2 and 3, the processor interconnect 25 "can be implemented as a system bus" (note column 7, lines 10-13).

Yamada et al. teach the function of the invention as presently claimed, but fail to specifically mention the act of assigning the addresses to the memories (in other words, each of the memories have been assigned addresses, as in the invention, but Yamada et al. do not disclose the specifics of how the address were put there).

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize a memory controller (with a requisite interface) in order to assign addresses to each of the units in Yamada et al., since (1) the addresses were assigned to each memory and something had to put them there, (2) there was no way that the addresses could have been pre-assigned at manufacture -- there must have been some control circuitry to assign address dynamically, since the Yamada et al. PMs were designed to be part of the type of large multiprocessor systems (which are constantly being reconfigured as units are added or deleted), (3) the memory control circuitry would have had to be sophisticated enough to provide *unique* global addresses

for each object in the network and (4) the dynamic address assignment would have been critical to speeding up message passing (the need for speed was clearly emphasized by the use of asynchronous message passing in Yamada et al.)

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (703) 305-3824. The examiner is generally available on alternate weekdays from 11:00 am to 9:00 pm, EST, and on weekends.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached at (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239 (Official communications)

or:

(703) 746-7240 (for Informal or Draft communications)

or:

(703) 746-7238 (for After-Final communications)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

B. James Peikari
Primary Examiner
Art Unit 2186

December 15, 2002

Interview Summary

Application No.	Applicant(s)
09/737,218	Norman et al.
Examiner	**Art Unit**
B. James Peikari	2186

All participants (applicant, applicant's representative, PTO personnel):

(1) *B. James Peikari* (3) _____

(2) *Dan Kluth (#32,146)* (4) _____

Date of Interview *Dec 16, 2002*

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy is given to 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No. If yes, brief description:

Claim(s) discussed: *1-3, 25, 47, 55-59 and 61*

Identification of prior art discussed:
N/A

Agreement with respect to the claims f)☒ was reached. g)☐ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments:
Applicant had not received the restriction requirement mailed on September 17, 2001.

Applicant elected Group I, claims 1-3.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

i)☐ It is not necessary for applicant to provide a separate record of the substance of the interview (if box is checked).

Unless the paragraph above has been checked, THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN ONE MONTH FROM THIS INTERVIEW DATE TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

_____
Examiner's signature, if required

Notice of References Cited

Application/Control No.	Applicant(s)/Patent Under Reexamination	
09/737,218	NORMAN ET AL.	
Examiner	Art Unit	Page 1 of 1
B. James Peikari	2186	

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,617,537	04-1997	Yamada et al.	709/214
	B	US-5,551,053	08-1996	Nadolski et al.	710/9
	C	US-5,412,788	05-1995	Collins et al.	711/157
	D	US-4,293,910	10-1981	Flusche et al.	711/157
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Form 1449*	Atty. Docket No.: 703.070US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Robert D. Norman	
	Filing Date: Herewith	Group: ~~Unknown~~ 2186

U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
BJP	5,029,209	07/02/1991	Strong, Jr., F.S., et al	~~380~~	~~25~~	06/13/90
BJP	5,293,498	03/08/1994	Iwatsubo, M.	~~395~~	~~325~~	04/19/93
BJP	5,430,859	07/04/1995	Norman, R.D., et al.	~~395~~	~~425~~	07/26/91
BJP	5,627,784	05/06/1997	Roohparvar, F.F.	365	189.01	07/28/95
BJP	5,640,332	06/17/1997	Baker, D.C., et al.	~~364~~	~~514A~~	05/16/96
BJP	5,687,117	11/11/1997	Chevallier, C.J., et al.	365	185.12	02/23/96
BJP	5,873,123	02/16/1999	Patel, R.B., et al.	711	202	06/25/96

FOREIGN PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes	No

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

**Examiner Initial	
BJP	"Draft Standard for A High-Speed Memory Interface (SyncLink)", Microprocessor and Microcomputer Standards Subcommittee of the IEEE Computer Society, New York: Institute of Electrical and Electronics Engineers, Inc., 1-52, (1996)

Examiner	Date Considered
Peikari	12/15/02

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.